Claims:

1. A method of applying a three-dimensional discrete wavelet transformation (DWT) to a plurality of video images, said plurality comprising frames, and said frames comprising rows and columns, said method comprising:

producing a plurality of blocks of DWT coefficients by:

respectively and successively filtering along a sequence of frames, a sequence of columns and a sequence of rows of the plurality of video images;

after applying each filter operation, subsampling the result of applying the filter operation; and

after producing the blocks of DWT coefficients, applying a bit-based conditional coding to embedded zero tree code the DWT coefficients.

2. The method of claim 1, wherein subsampling comprises dropping alternate frames, alternate columns and alternate rows after corresponding filter operations.

3. The method of claim 1, wherein a plurality of blocks comprises eight blocks.

4. The method of claim 1, wherein applying a filter operation comprises, for each filter operation, applying one of a high pass filter and a low pass filter.

5. An integrated circuit comprising:

an architecture to apply a three-dimensional discrete wavelet transformation (DWT) to a plurality of video images and produce a plurality of blocks of DWT coefficients, said plurality comprising frames, and said frames comprising rows and columns;

said architecture adapted to (a) respectively and successively filter along a sequence of frames, a sequence of columns and a sequence of rows of the plurality of video images using, for each filter operation, one of a high pass and a low pass filter, (b) after applying each filter operation, subsample the result of applying the filter operation, and (c) after producing the blocks of DWT coefficients applying a bit-based conditional coding to embedded zero tree encode the DWT coefficients.

6. The integrated circuit of claim 5, wherein said architecture comprises at least one of the following: hardware, software, firmware, and any combination thereof.

7. The integrated circuit of claim 6, wherein said subsampling capability of

said architecture comprises being adapted to drop alternate frames, alternate columns and alternate rows after corresponding filter operations.

8. The integrated circuit of claim 6, wherein a plurality of blocks comprises eight blocks.

9. The integrated circuit of claim 6, wherein applying a filter operation comprises, for each filter operation, applying one of a high pass filter and a low pass filter.

10. A method of applying an inverse three-dimensional discrete wavelet transformation (3D IDWT) to a plurality of transformed video image sub-blocks, said sub-blocks comprising transformed frames, and said frames comprising rows and columns, said method comprising:

inverse transforming the sub-blocks of transformed video images by:

(1) applying a bit-based conditional decoding to the embedded zero tree encoded DWT coefficients of the block to obtain a DWT coefficient matrix;

(2) up-sampling respective sub-blocks of the DWT coefficient matrix by row, column and frame;

(3) filtering and combining one or more respective pairs of up-

sampled sub-blocks to produce an up-sampled sub-block corresponding to each respective pair;

(4) reapplying (3) to any produced up-sampled sub-block pairs until one up-sampled sub-block remains;

(5) multiplying the one remaining up-sampled sub-block by eight to produce a block at the next higher resolution.

11. The method of claim 10, wherein the respective sub-blocks of the DWT matrix comprise eight sub-blocks.

12. The method of claim 10, wherein filtering and combining one or more respective pairs of up-sampled sub-blocks comprises applying an inverse low-pass filter to one up-sampled sub-block of the pair and applying a high-pass filter to the other up-sampled sub-block of the pair.

13. The method of claim 10, wherein up-sampling comprises inserting alternate frames, alternate columns and alternate rows.

14. An integrated circuit comprising:

an architecture to apply an inverse three-dimensional discrete wavelet transformation (3D IDWT) to a plurality of transformed video image sub-blocks,

said sub-blocks comprising transformed frames, and said frames comprising rows and columns;

said architecture adapted to inverse transforming the sub-blocks of transformed video images by:

(a) applying a bit-based conditional decoding to the embedded zero tree encoded DWT coefficients of the block to obtain a DWT coefficient matrix; (b) up-sampling respective sub-blocks of the DWT coefficient matrix by row, column and frame; (c) filtering and combining one or more respective pairs of up-sampled sub-blocks to produce an up-sampled sub-block corresponding to each respective pair; (d) reapplying (c) to any produced up-sampled sub-block pairs until one up-sampled sub-block remains; and (e) multiplying the one remaining up-sampled sub-block by eight to produce a block at the next higher resolution.

15. The integrated circuit of claim 14, wherein said architecture comprises at least one of the following: hardware, software, firmware, and any combination thereof.

16. The integrated circuit of claim 15, wherein the respective sub-blocks of the DWT coefficient matrix comprise eight sub-blocks.

17. The integrated circuit of claim 15, wherein filtering and combining one or more respective pairs of up-sampled sub-blocks comprises applying an inverse low-pass filter to one up-sampled sub-block of the pair and applying a high-pass filter to the other up-sampled sub-block of the pair.

18. The integrated circuit of claim 15, wherein up-sampling comprises inserting alternate frames, alternate columns and alternate rows.

19. An article comprising: a storage medium having stored thereon instructions, said instructions, when executed by a computing platform, resulting in applying a three-dimensional discrete wavelet transformation (DWT) to a plurality of video images, said plurality comprising frames, and said frames comprising rows and columns, by:

producing a plurality of blocks of DWT coefficients by:

respectively and successively filtering along a sequence of frames, a sequence of columns and a sequence of rows of the plurality of video images;

after applying each filter operation, subsampling the result of applying the filter operation; and

after producing the blocks of DWT coefficients, applying a bit-based conditional coding to embedded zero tree code the DWT coefficients.

20. The article of claim 19, wherein the plurality of sub-blocks comprises eight sub-blocks.

21. The article of claim 19, wherein filtering and combining one or more respective pairs of up-sampled sub-blocks comprises applying an inverse low-pass filter to one up-sampled sub-block of the pair and applying a high-pass filter to the other up-sampled sub-block of the pair.

22. An article comprising: a storage medium having stored thereon instructions, said instructions, when executed by a computing platform, resulting in applying an inverse three-dimensional discrete wavelet transformation (3D IDWT) to a plurality of transformed video image sub-blocks, said sub-blocks comprising transformed frames, and said frames comprising rows and columns, by:

(1) applying a bit-based conditional decoding to the embedded zero tree encoded DWT coefficients of the block to obtain a DWT coefficient matrix;

(2) up-sampling respective sub-blocks of the DWT coefficient matrix by row, column and frame;

(3) filtering and combining one or more respective pairs of up-sampled sub-blocks to produce an up-sampled sub-block

corresponding to each respective pair;

(4) reapplying (3) to any produced up-sampled sub-block pairs until one up-sampled sub-block remains; and

(5) multiplying the one remaining up-sampled sub-block by eight to produce a block at the next higher resolution.

23. The article of claim 22, wherein the respective sub-blocks of the DWT coefficient matrix comprise eight sub-blocks.

24. The article of claim 22, wherein filtering and combining one or more respective pairs of up-sampled sub-blocks comprises applying an inverse low-pass filter to one up-sampled sub-block of the pair and applying a high-pass filter to the other up-sampled sub-block of the pair.

25. A system comprising:

an integrated circuit, a memory, and a bus coupling said integrated circuit and memory;

wherein said integrated circuit includes an architecture to apply a three-dimensional discrete wavelet transformation (DWT) to a plurality of video images and produce a plurality of blocks of DWT coefficients, said plurality comprising frames, and said frames comprising rows and columns;

said architecture adapted to (a) respectively and successively filter along a sequence of frames, a sequence of columns and a sequence of rows of the plurality of video images using, for each filter operation, one of a high pass and a low pass filter, (b) after applying each filter operation, subsample the result of applying the filter operation, and (c) after producing the blocks of DWT coefficients applying a bit-based conditional coding to embedded zero tree encode the DWT coefficients.

26. The system of claim 25, wherein said architecture comprises at least one of the following: hardware, software, firmware, and any combination thereof.

27. The system of claim 26, wherein said subsampling capability of said architecture comprises being adapted to drop alternate frames, alternate columns and alternate rows after corresponding filter operations.

28. The system of claim 26, wherein a plurality of blocks comprises eight blocks.

29. The system of claim 26, wherein applying a filter operation comprises, for each filter operation, applying one of a high pass filter and a low pass filter.

30. A system comprising:

an integrated circuit, a memory, and a bus coupling said integrated circuit and memory;

wherein said integrated circuit comprises an architecture to apply an inverse three-dimensional discrete wavelet transformation (3D IDWT) to a plurality of transformed video image sub-blocks, said sub-blocks comprising transformed frames, and said frames comprising rows and columns;

said architecture adapted to inverse transforming the sub-blocks of transformed video images by:

(a) applying a bit-based conditional decoding to the embedded zero tree encoded DWT coefficients of the block to obtain a DWT coefficient matrix; (b) up-sampling respective sub-blocks of the DWT coefficient matrix by row, column and frame; (c) filtering and combining one or more respective pairs of up-sampled sub-blocks to produce an up-sampled sub-block corresponding to each respective pair; (d) reapplying (c) to any produced up-sampled sub-block pairs until one up-sampled sub-block remains; and (e) multiplying the one remaining up-sampled sub-block by eight to produce a block at the next higher resolution.

31. The system of claim 30, wherein said architecture comprises at least one of the following: hardware, software, firmware, and any combination thereof.

32. The system of claim 31, wherein the respective sub-blocks of the DWT coefficient matrix comprise eight sub-blocks.

33. The system of claim 31, wherein filtering and combining one or more respective pairs of up-sampled sub-blocks comprises applying an inverse low-pass filter to one up-sampled sub-block of the pair and applying a high-pass filter to the other up-sampled sub-block of the pair.

34. The system of claim 31, wherein up-sampling comprises inserting alternate frames, alternate columns and alternate rows.